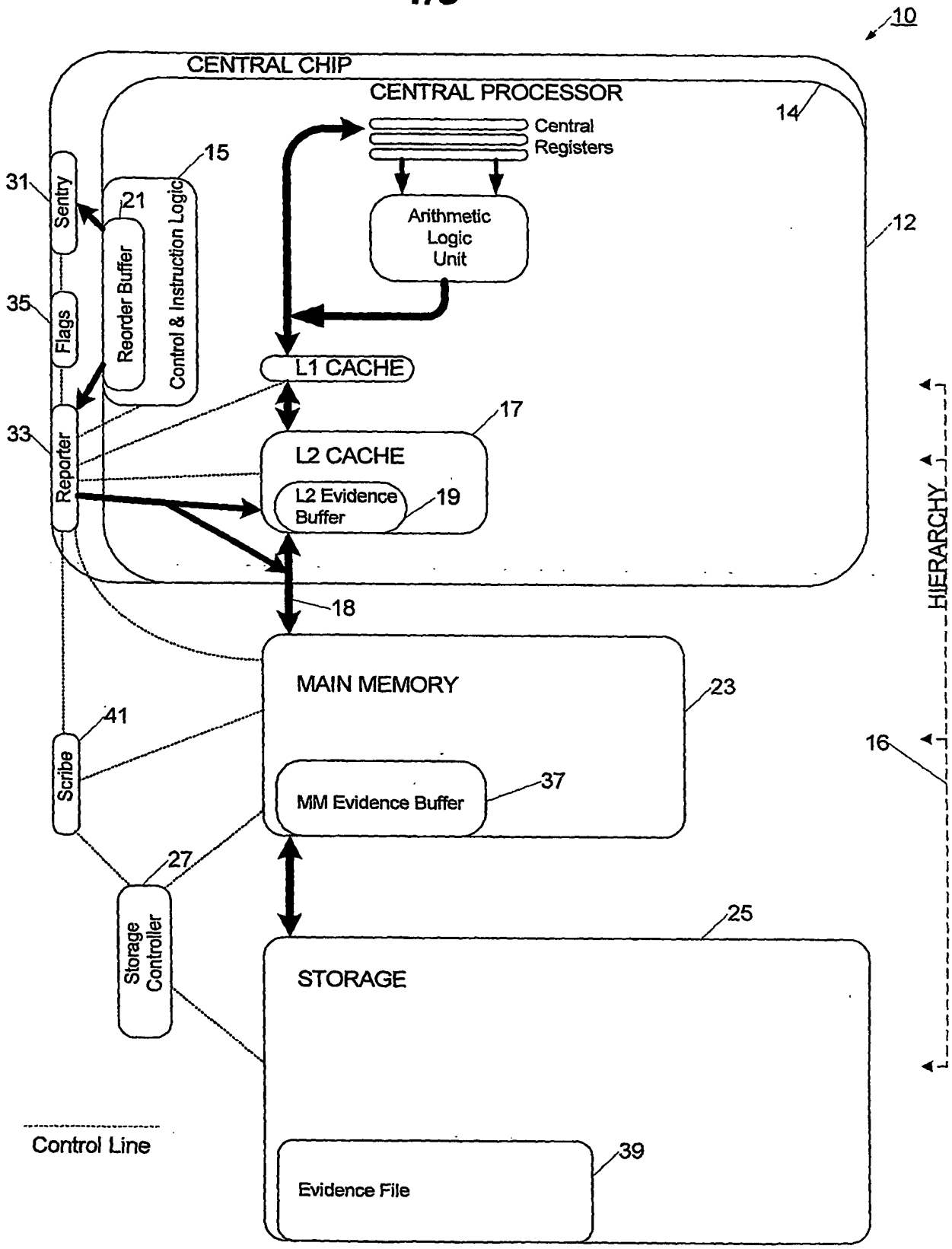
10
CENTRAL CHIP
CENTRAL PROCESSOR
14
Central Registers
Arithmetic Logic Unit
12
15
Control & Instruction Logic
21
Reorder Buffer
31
Sentry
35
Flags
33
Reporter
L1 CACHE
17
L2 CACHE
L2 Evidence Buffer
19
18
HIERARCHY
MAIN MEMORY
23
41
Scribe
16
MM Evidence Buffer
37
27
Storage Controller
25
STORAGE
Control Line
39
Evidence File

FIG. 1

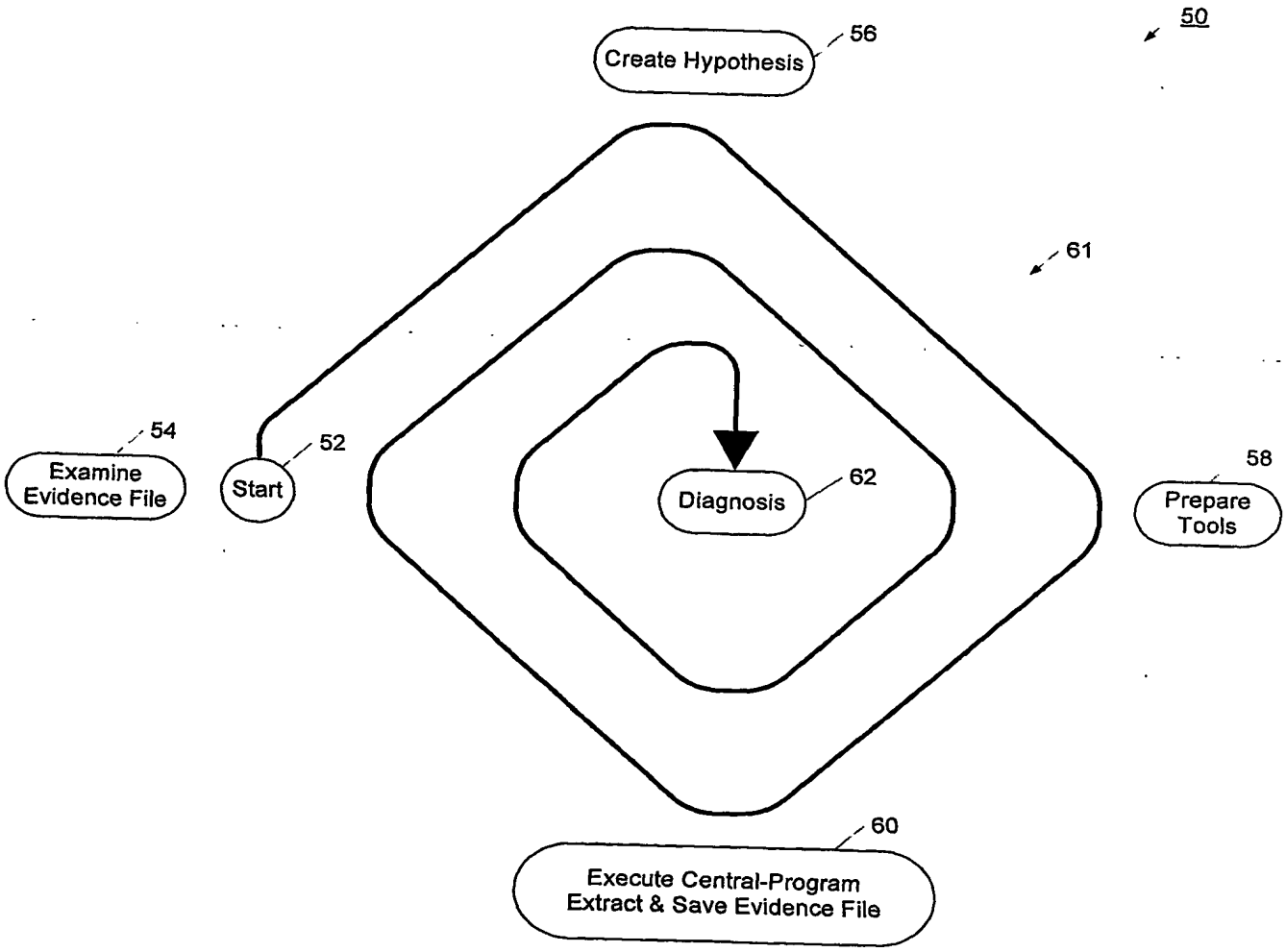
50
Create Hypothesis
56
61
54
Examine Evidence File
52
Start
Diagnosis
62
58
Prepare Tools
60
Execute Central-Program Extract & Save Evidence File

FIG. 2

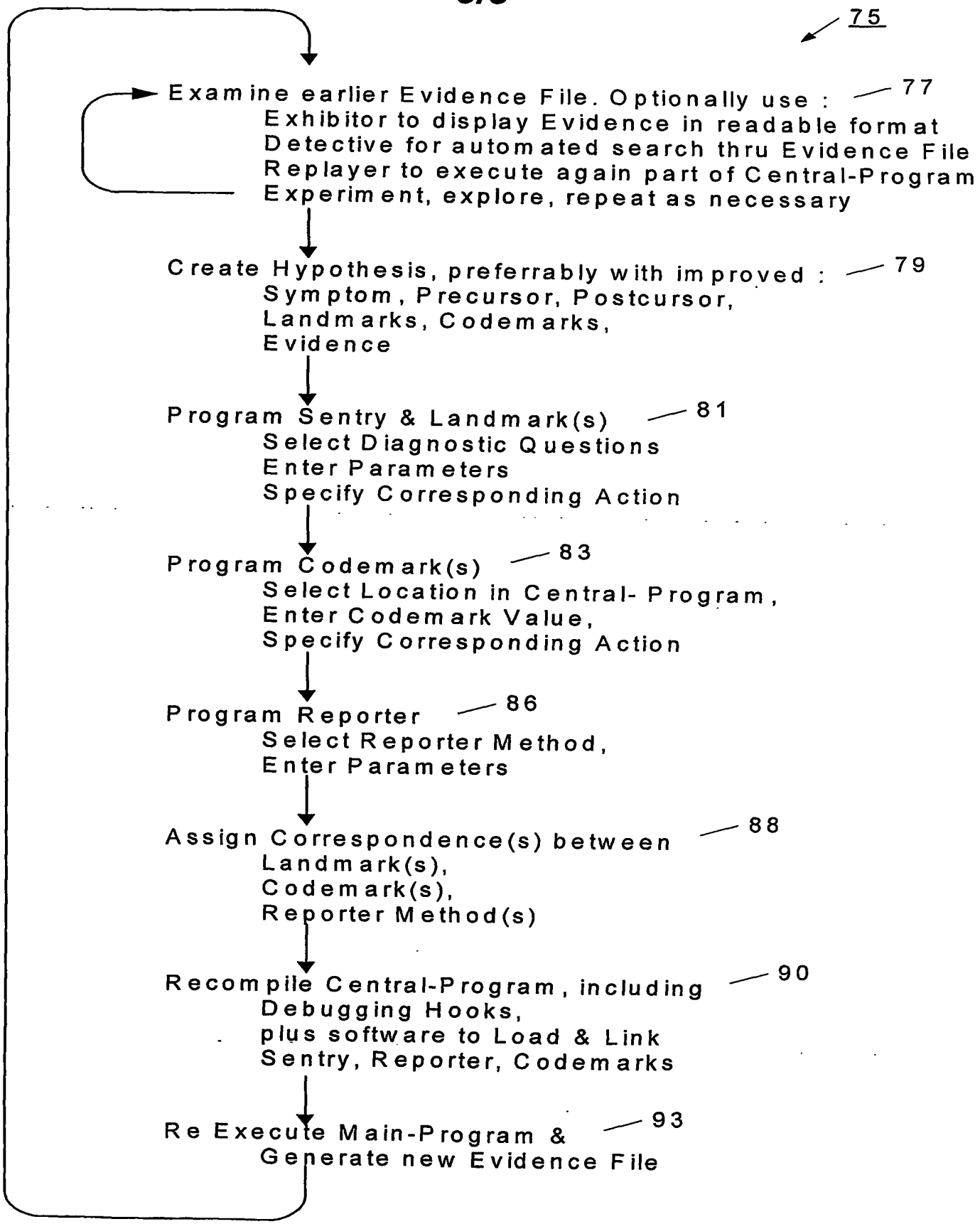
75
Examine earlier Evidence File. Optionally use :
77
Exhibitor to display Evidence in readable format
Detective for automated search thru Evidence File
Replayer to execute again part of Central-Program
Experiment, explore, repeat as necessary
Create Hypothesis, preferrably with improved :
79
Symptom, Precursor, Postcursor,
Landmarks, Codemarks,
Evidence
Program Sentry & Landmark(s)
81
Select Diagnostic Questions
Enter Parameters
Specify Corresponding Action
Program Codemark(s)
83
Select Location in Central- Program,
Enter Codemark Value,
Specify Corresponding Action
Program Reporter
86
Select Reporter Method,
Enter Parameters
Assign Correspondence(s) between
88
Landmark(s),
Codemark(s),
Reporter Method(s)
Recompile Central-Program, including
90
Debugging Hooks,
plus software to Load & Link
Sentry, Reporter, Codemarks
Re Execute Main-Program &
93
Generate new Evidence File

FIG. 3

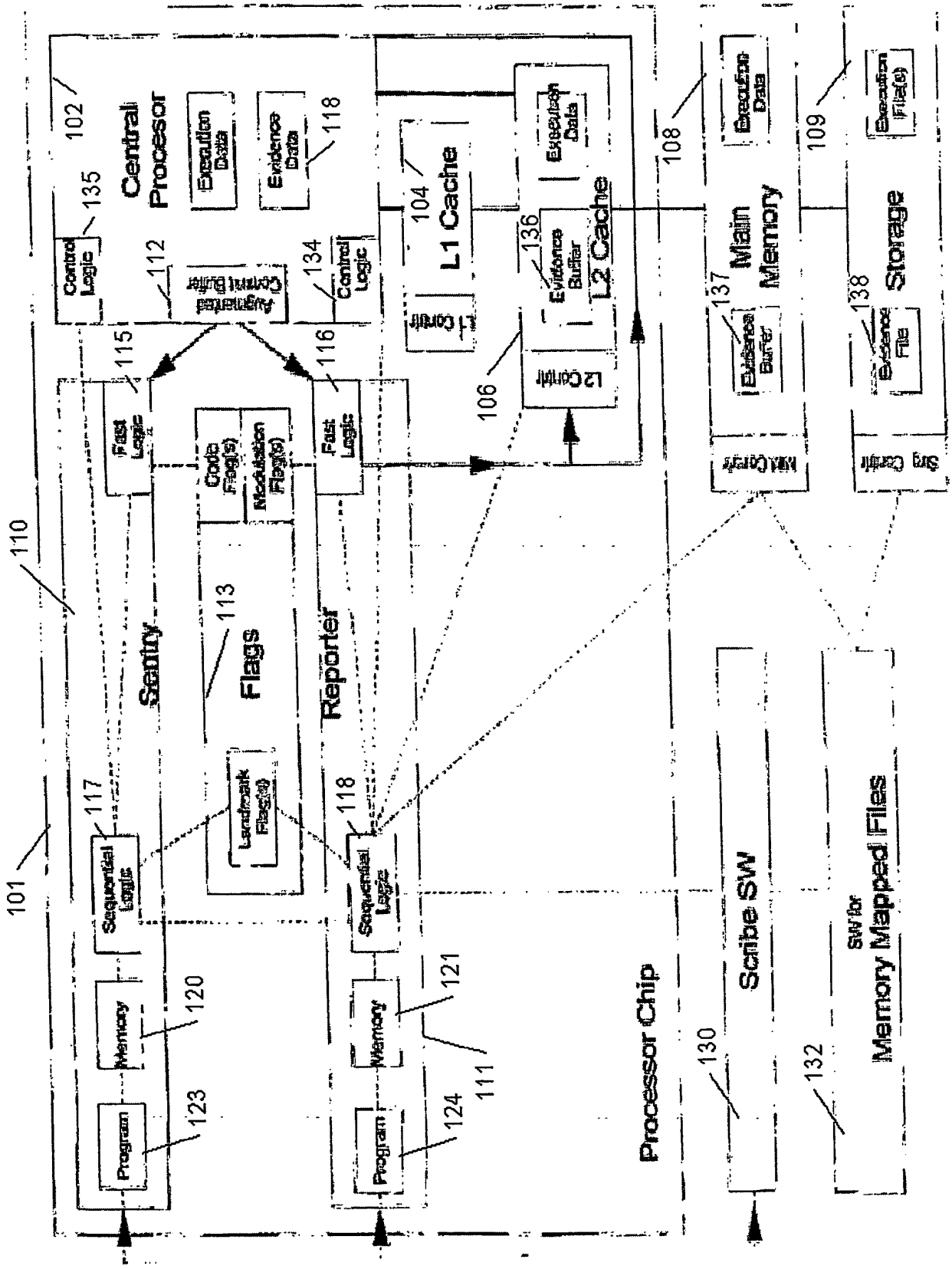
Central Processor
Execution Data
Evidence Data
Control Logic
Control Buffer
L1 Cache
L2 Cache
Evidence Buffer
Main Memory
Storage
Fast Logic
Code Flag(s)
Modification Flag(s)
Sentry
Flags
Reporter
Landmark Flag(s)
Sequential Logic
Memory
Program
Processor Chip
Scribe SW
SW for Memory Mapped Files
Execution Files(s)
Evidence File
101
102
104
106
108
109
110
111
112
113
115
116
117
118
120
121
123
124
130
132
134
135
136
137
138

FIG. 4

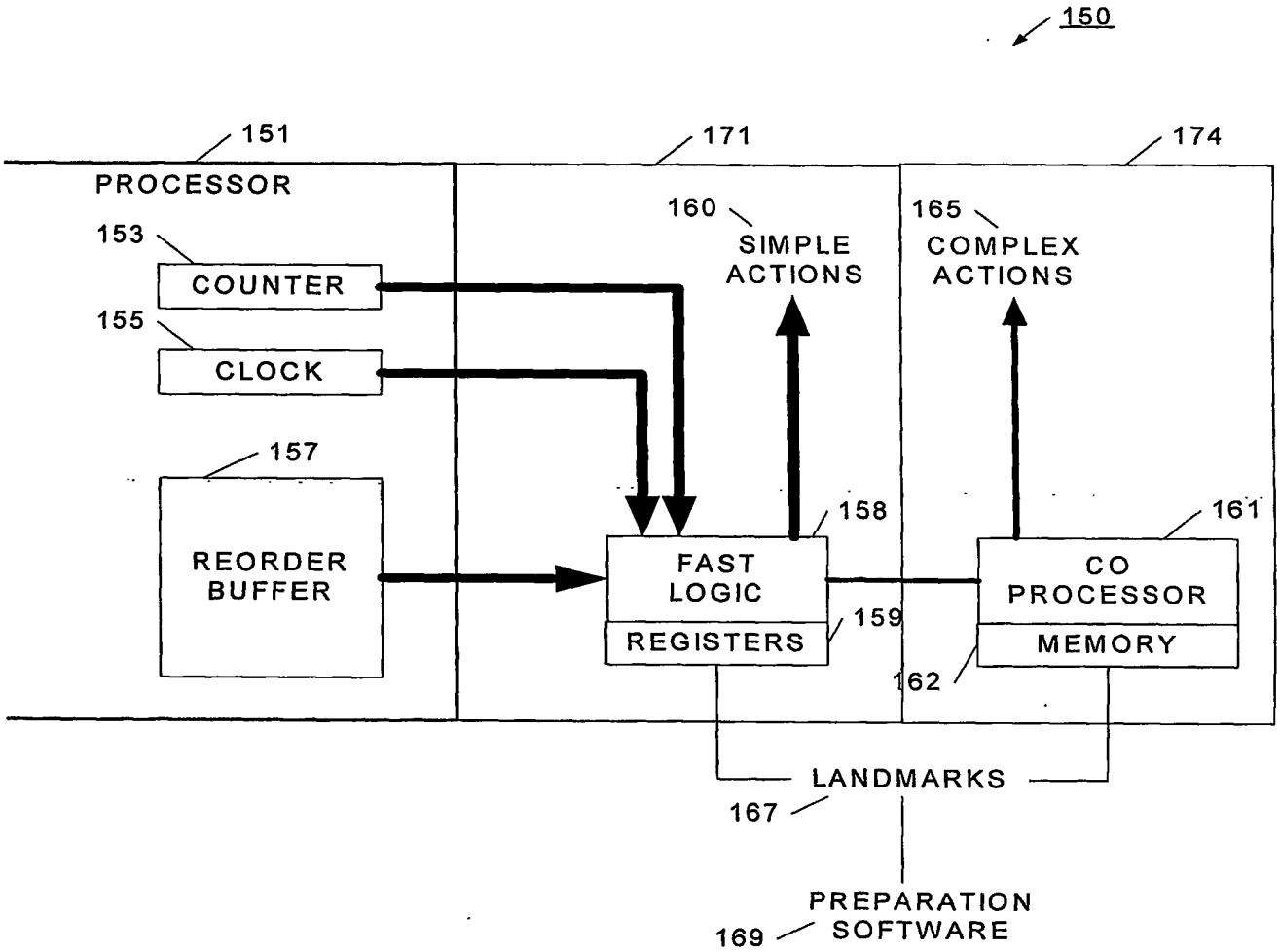
150
151
PROCESSOR
171
174
160
SIMPLE ACTIONS
165
COMPLEX ACTIONS
153
COUNTER
155
CLOCK
157
REORDER BUFFER
158
FAST LOGIC
159
REGISTERS
161
CO PROCESSOR
MEMORY
162
LANDMARKS
167
PREPARATION SOFTWARE
169

FIG. 5

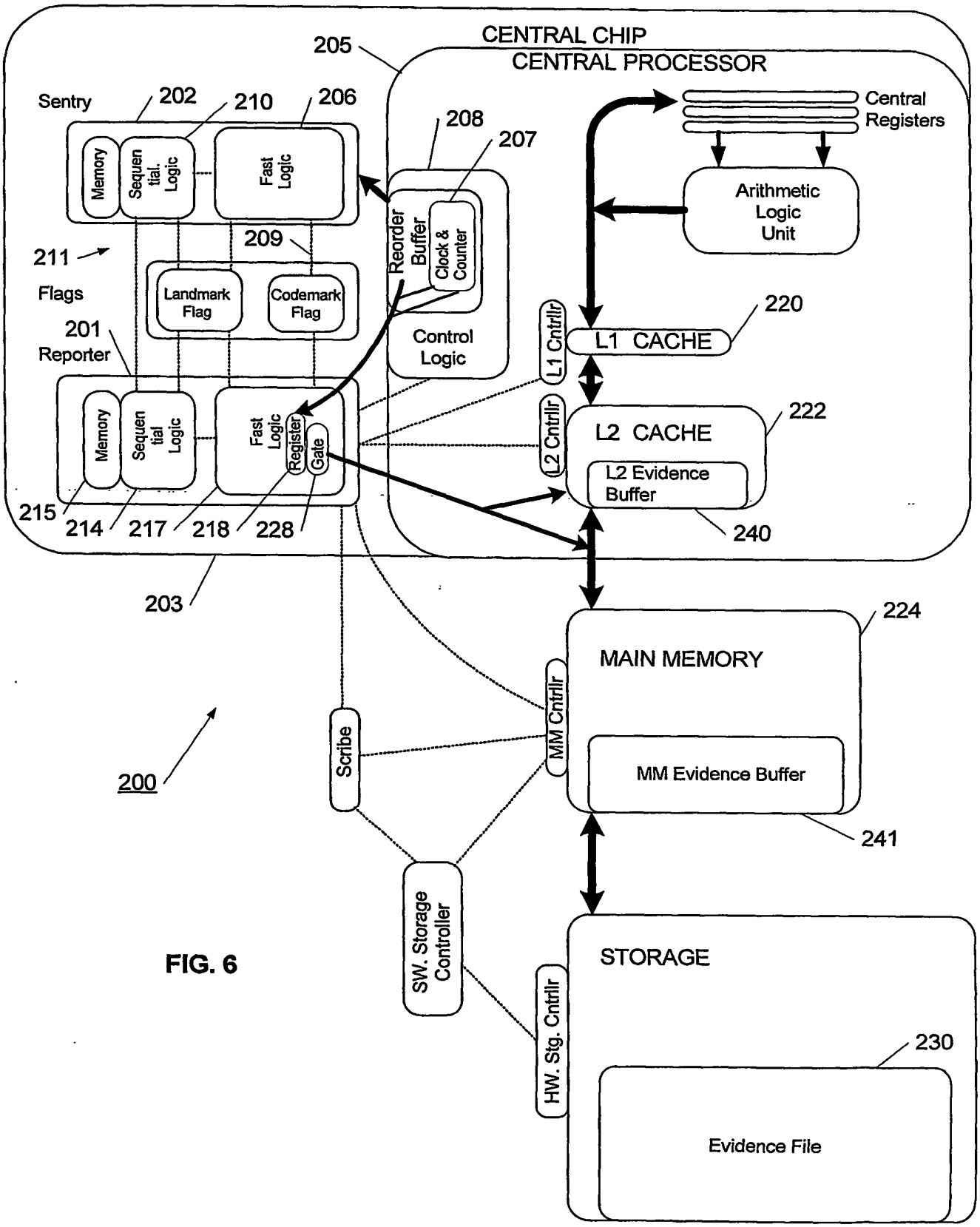
CENTRAL CHIP
205
CENTRAL PROCESSOR
Sentry
202
210
206
Memory
Sequen tial Logic
Fast Logic
208
207
Reorder Buffer
Clock & Counter
Control Logic
Central Registers
Arithmetic Logic Unit
209
211
Flags
Landmark Flag
Codemark Flag
201
Reporter
L1 Cntrllr
220
L1 CACHE
L2 Cntrllr
222
L2 CACHE
L2 Evidence Buffer
240
Register
Gate
215
214
217
218
228
203
224
MAIN MEMORY
MM Cntrllr
MM Evidence Buffer
241
Scribe
200
SW. Storage Controller
STORAGE
HW. Stg. Cntrllr
230
Evidence File

FIG. 6

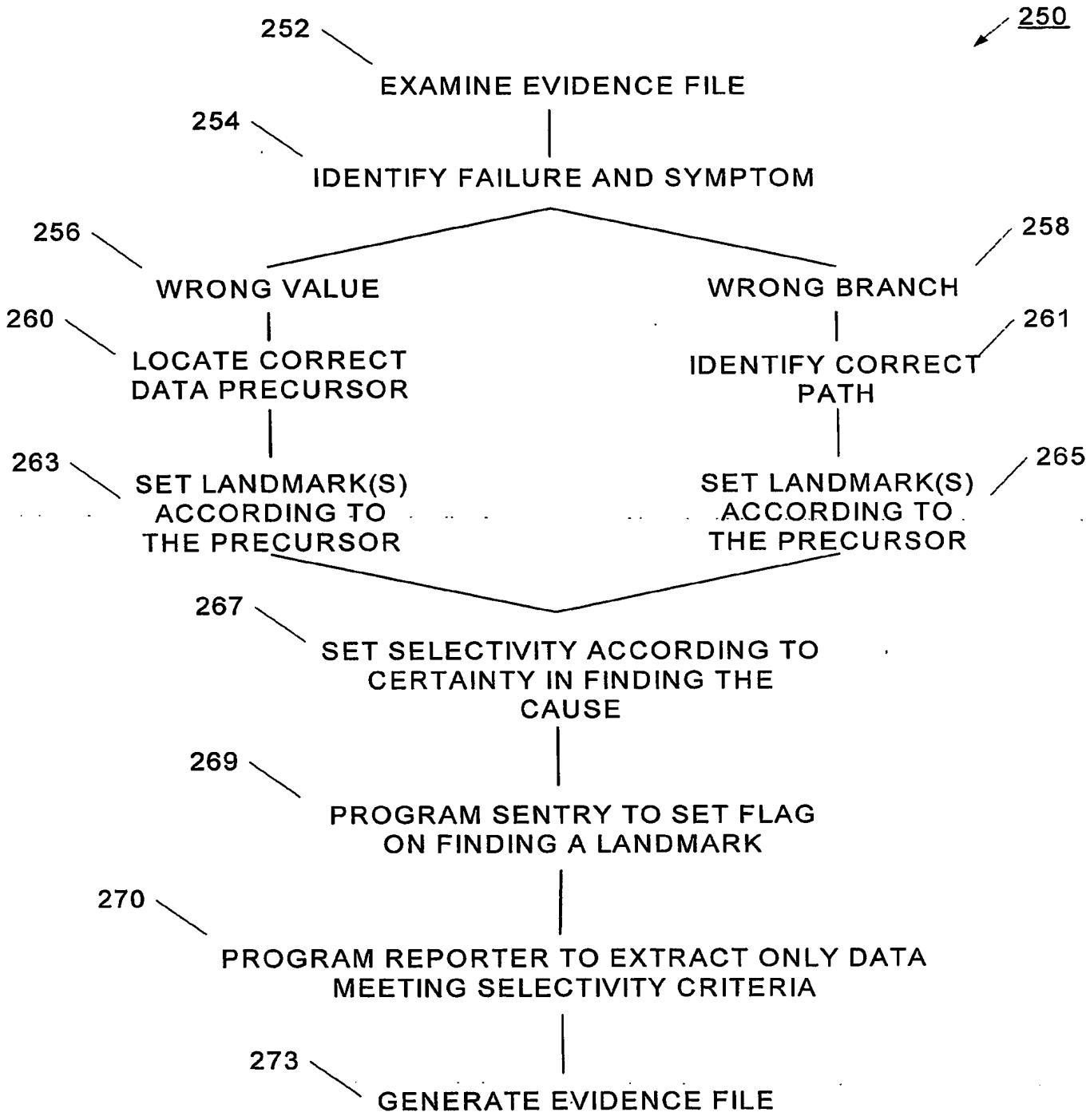
250
252
EXAMINE EVIDENCE FILE
254
IDENTIFY FAILURE AND SYMPTOM
256
WRONG VALUE
258
WRONG BRANCH
260
LOCATE CORRECT DATA PRECURSOR
261
IDENTIFY CORRECT PATH
263
SET LANDMARK(S) ACCORDING TO THE PRECURSOR
265
SET LANDMARK(S) ACCORDING TO THE PRECURSOR
267
SET SELECTIVITY ACCORDING TO CERTAINTY IN FINDING THE CAUSE
269
PROGRAM SENTRY TO SET FLAG ON FINDING A LANDMARK
270
PROGRAM REPORTER TO EXTRACT ONLY DATA MEETING SELECTIVITY CRITERIA
273
GENERATE EVIDENCE FILE

FIG. 7

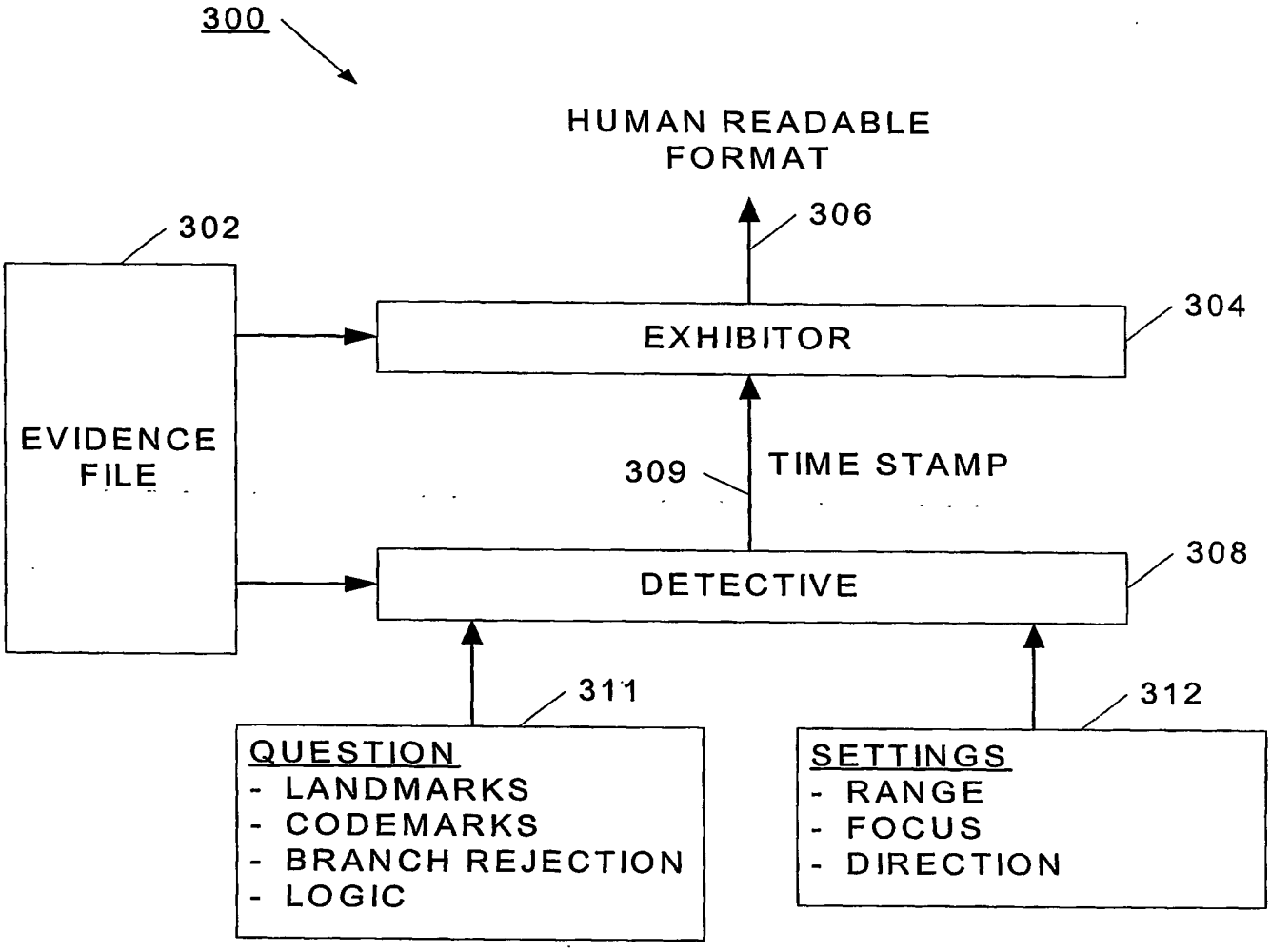
300
HUMAN READABLE FORMAT
306
302
304
EXHIBITOR
EVIDENCE FILE
309
TIME STAMP
308
DETECTIVE
311
312
QUESTION
- LANDMARKS
- CODEMARKS
- BRANCH REJECTION
- LOGIC
SETTINGS
- RANGE
- FOCUS
- DIRECTION

FIG. 8